

Abstract of the Disclosure:

A semiconductor unit constituting a memory device has a memory chip, a package substrate having three wiring layers. Power-supply surfaces (VDD surface) and (GND surface) are wired on the package substrate while an intra-package DQ bus is wired on an intermediate layer between both of the power-supply surfaces. The memory device has two DQ pins every one intra-package DQ bus. The intra-package DQ bus is connected to a signal terminal pad of the memory chip through a via hole. In view of the two DW pins, a via hole for connecting the intra-package DQ bus with the signal terminal pad constitutes a branch wire.